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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,815	06/11/2001	Hassan S. Hashemi	00CON159PC-CIP1	3172

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EXAMINER

COSTANZO, PATRICIA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/878,815

Applicant(s)

HASHEMI ET AL.

Examiner

Patricia M. Costanzo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-71 is/are pending in the application.
- 4a) Of the above claim(s) 56-71 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-55 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 and 8 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 28 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Both Claims 28 and Claim 30 recite that – said second via (defined in Claim 26 as vias (126) or (130)) provides an electrical connection between said semiconductor die and said heat spreader (148). However, Figure 1 shows no such electrical connection. Does Applicant mean to say “first via”, as defined by Claim 21, instead of “second via”?

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily

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published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 – 6, are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,377,464 (Hashemi *et al.*).

Referring to Claim 1: Hashemi *et al.* disclose a structure comprising:

- a substrate (Figure 6 (608) having a top surface for receiving a die (Figure 6 (602);

- a printed circuit board (see, for example, Col. 12, lines 9 – 12 and 29 - 32) attached to a bottom surface of said substrate;

- at least one via (Figure 6 (606a)) in said substrate;

- said at least one via providing an electrical connection between a signal bond pad (which is located on the chip at the chip end of signal wire (622) as illustrated in Figure 6) of said die and said printed circuit board (which is not illustrated but is taught, see above).

Referring to Claims 2, 3, 4, and 5: Hashemi *et al.* disclose a structure, as recited above,

- further disclosing a semiconductor die (Figure 6 (602), an organic substrate (Col. 4, line 21), wherein the organic substrate is FR4 based laminate (Col. 4, lines 26 – 31, and a ceramic substrate (Col. 3, lines 20 – 21).

Referring to Claim 6: Hashemi *et al.* disclose a structure, as recited above, further

- disclosing wherein said at least one via (Figure 6, via that is under substrate bond pad (632)) provides an electrical connection between a substrate bond pad

(632) and said printed circuit board (not shown, discussed above), wherein said substrate bond pad is electrically connected to said signal bond pad (at die end of wire (622) of said die.

Referring to 7: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said at least one via (*i.e.*, the via that is connected to signal bond pads in Figure 6) abuts said substrate bond pad (632).

Referring to Claim 8: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein the substrate bond pad Figure 6 (632) is electrically connected to said signal bond pad of said die by a signal bonding wire (Figure 6 (622)).

Referring to Claim 9: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) provides an electrical connection between said signal bond pad (denoted by 730) of said die (710) and a land (714), said land being electrically connected to said printed circuit board (not shown but discussed above).

Referring to Claim 10: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) abuts said land (714).

Referring to Claim 11: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) provides an electrical connection between a substrate bond pad (pad on substrate, not specifically

illustrated, but indicated as connection between substrate and wire (730)) and a land (714), wherein said substrate bond pad is electrically connected to said signal bond pad of said die (pad on die, not specifically illustrated, but indicated as connection between wire (730) and die (710)).

Referring to Claim 12: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) abuts said substrate bond pad (see above) and said land (714).

Referring to Claims 13 and 14: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said substrate bond pad is electrically connected to said signal bond pad of said die by a signal bonding wire (Figure 7 (730)).

Referring to Claims 15 and 16: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said at least one via (Figure 7 (708)) comprises copper (Col.4. lines 31 – 32 in conjunction with Col. 5, lines 40 – 44 and Col. 6, lines 29 - 32).

Referring to Claims 17 - 19 and 27: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein a heat spreader is attached to bottom surface of substrate and said first via (see, for example, Figure 7 (708)) providing a connection between said semiconductor die and said heat spreader (see, for example, Col. 6, lines 10 – 30; note: Figure 6 illustrates an analogous arrangement) wherein said heat spreader is an electrical conductor (Col. 6, lines

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19 – 20) and where said heat spreader is attached to a printed circuit board (Col. 7, lines 2 – 5).

Referring to Claim 20: Hashemi *et al.* disclose a structure, as recited above, further comprising a substrate down bond area attached to said top surface of said substrate (Figure 7, downbonds (730)) connected to die attach pad (732), see also Col. 7, line 41 – 42).

Referring to Claim 21: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said first via (Figure 7 (708) provides an electrical connection between said substrate down bond area (732) and said heat spreader (that is connected to (714) (see above).

Referring to Claim 22: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein a semiconductor die (Figure 7 (710)) ground bond pad on said semiconductor die is electrically connected to said substrate down bond area) by a down bonding wire (730) (see also, Col. 7 lines 41 – 42).

Referring to Claims 23 and 24: Hashemi *et al.* disclose a structure, as recited above, including the limitations recited in Claims 23 and 24 (see above).

Referring to Claim 25: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said heat spreader is attached to a printed circuit board by solder (see, for example, Col. 3, lines 17 – 21).

Referring to Claim 26: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein a second via (Figure 6 (606) not referenced by connected to bond pad (632)) provides an electrical connection (wires (622) between a signal bond pad of said semiconductor die (602) and a printed circuit board substrate down bond area (as discussed above).

Referring to Claims 28 and 30, as far as Claims 28 and 30 are in compliance with 35 U.S.C. 112, 2nd paragraph, and as well as indefinite claims can be understood, Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said “first” via (Figure 6 (606a) provides an electrical connection between said semiconductor die (602) and said heat spreader (that is connected to (610), see above).

Referring to Claims 29, 31, 32, 33, 36, and 38: Hashemi *et al.* disclose a structure, as recited above, including the limitations recited in Claims 29, 31, 32, 33, 36, and 38 (see above).

Referring to Claims 34, 37, and 39: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said second via (Figure 6 (606) as discussed above) provides an electrical connection (wires (622) or (620)) between a substrate bond pad (632) and a land (not illustrated in Figure 6 but taught in Col. 12, lines 18 – 24, and see Figure 5, lands (510)), wherein said substrate bond pad (Figure 6 (632) is electrically connected to said signal bond pad of said

semiconductor die (602) and wherein said land is electrically connected to said printed circuit board (as discussed above).

Referring to Claims 35 and 40: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said second via (Figure 6 (606) not referenced by connected to substrate bond pad (632)) abuts said substrate bond pad (632) and said land (not illustrated in Figure 6 but taught in Col. 12, lines 18 – 24, and see Figure 5, lands (510), as discussed above).

Referring to Claims 41 - 43: Hashemi *et al.* disclose a structure, as recited above, including the limitations disclosed in Claims 41 – 43.

Referring to Claim 44: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein a first plurality of vias (Figure 6, vias (606a – 606c)) providing a connection between said semiconductor die (602) and said heat spreader which is attached to ground conductive pads (610) as discussed above.

Referring to Claims 45 and 47 - 52: Hashemi *et al.* disclose a structure, as recited above, including the limitations disclosed in Claims 45 and 47 – 52.

Referring to Claim 46: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein a second plurality of vias (Figure 6, un-referenced vias (606)) providing a connection between a plurality of signal bond pads (not referenced but connected to wire (622)) of said semiconductor die (602) and said printed circuit board (as discussed above).

Referring to Claim 53: Hashemi *et al.* disclose a structure, as recited above, further disclosing wherein said second plurality of vias (Figure 6, un-referenced vias (606)) provide electrical connections between each one of said plurality of signal bond pads of said semiconductor die (602) and a respective one of a plurality of lands ((610) as taught in Col. 12, lines 18 – 24 which teaches using a plurality of exposed attachment pads), said plurality of lands being electrically connected to said printed circuit board (as discussed above).

Referring to Claims 54 - 55: Hashemi *et al.* disclose a structure, as recited above, including the limitations disclosed in Claims 54 – 55.

Conclusion

Any inquiry concerning this communication should be directed to Patricia Costanzo at 703 305 5675 on Monday – Friday from 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful Supervisory Primary Examiner Tom Thomas can be reached at 703 308 2772.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist at 703 308 0956.

Using facsimile machines to transmit correspondence is encouraged.

Papers may be faxed directly to Examiner at 703 745 2002.

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The official Technical Center 2800 before-final FAX number is 703 872 9318 and the after-final FAX number is 703 872 9319. These FAX numbers will provide the FAX sender with an auto-reply verifying receipt of their FAX by the United States Patent and Trademark Office. If there should be a problem while faxing to the Office, please contact Technical Center 2800 Customer Service at 703 306 3329.

pmc
July 3, 2002


Sara Crane
Primary Examiner